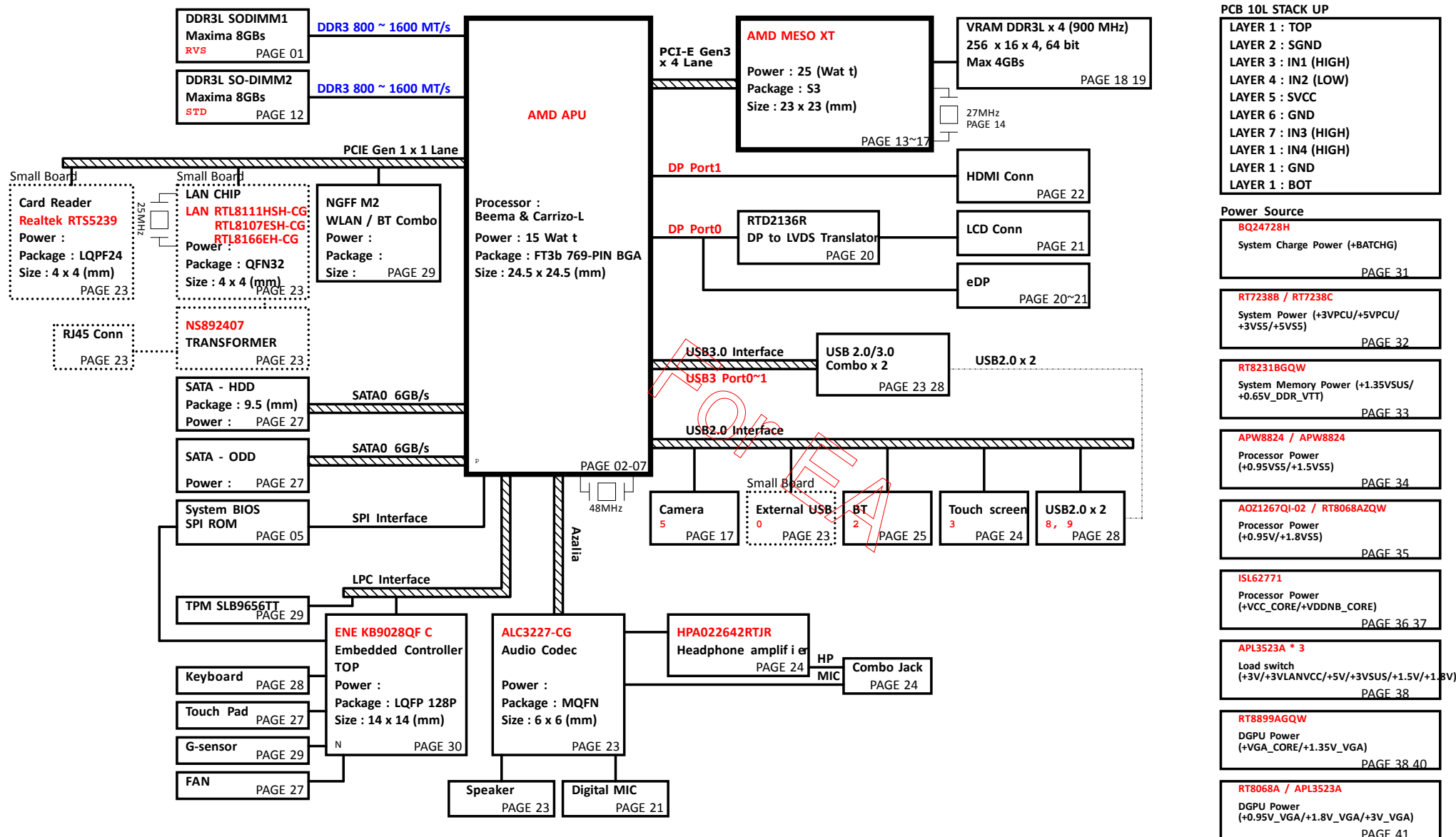
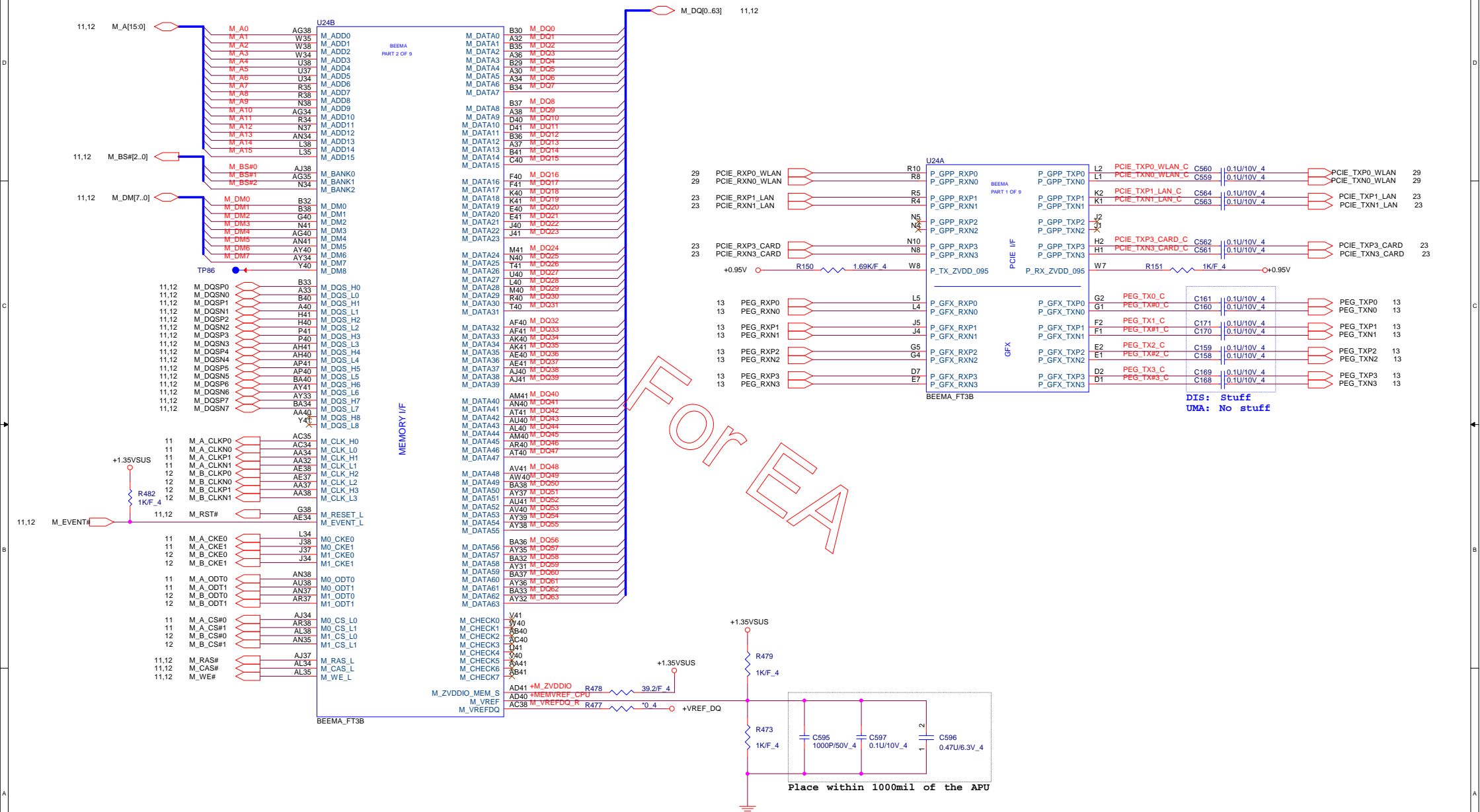
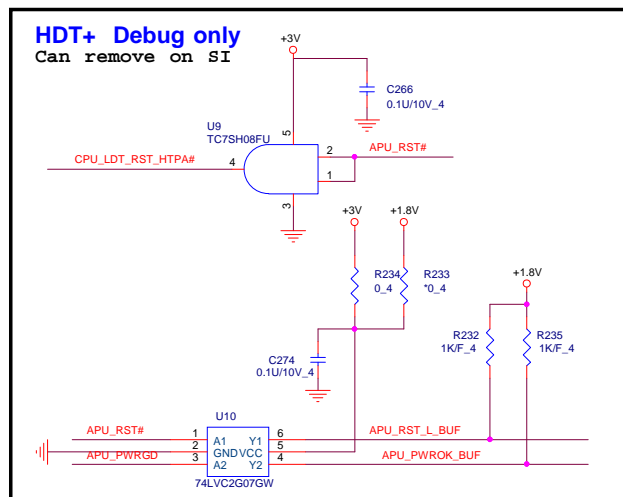
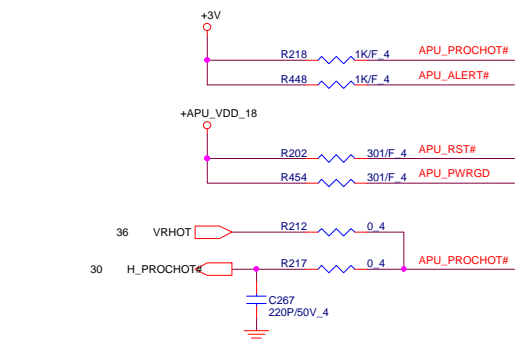


# Chocolate AMD Beema DIS/UMA (14.0"/15.6"/17.3")







### MV co-layout Kabini

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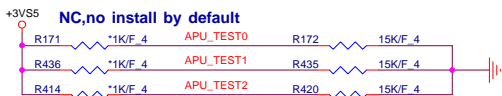
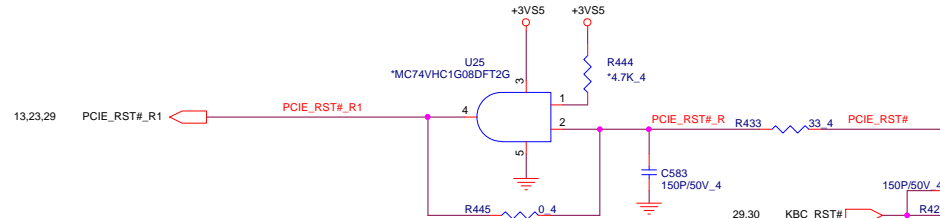
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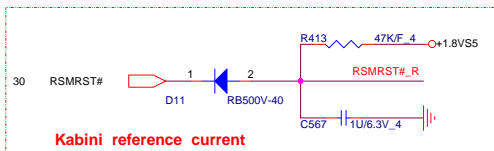
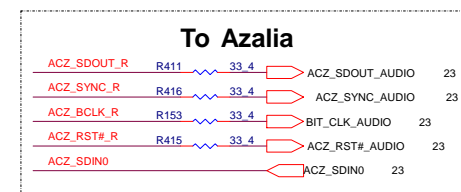
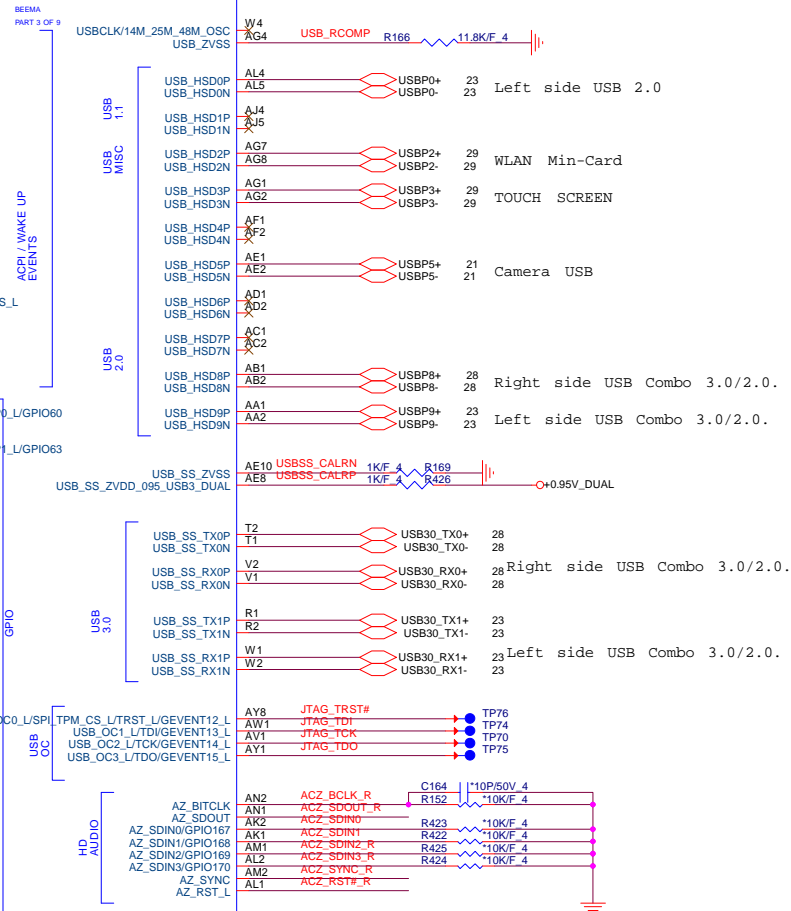
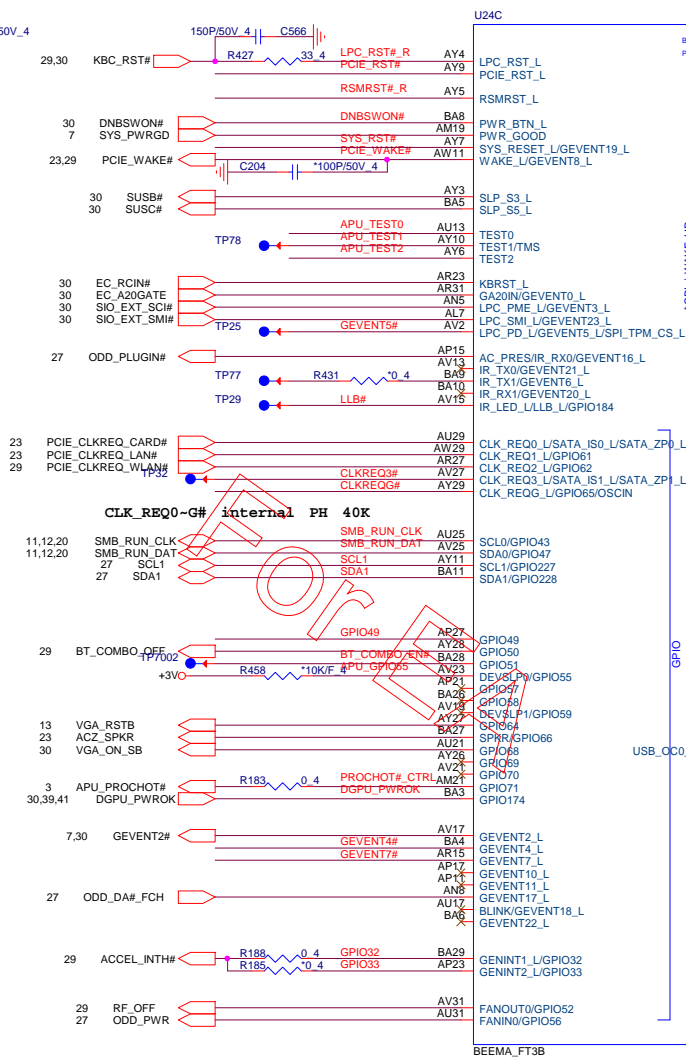
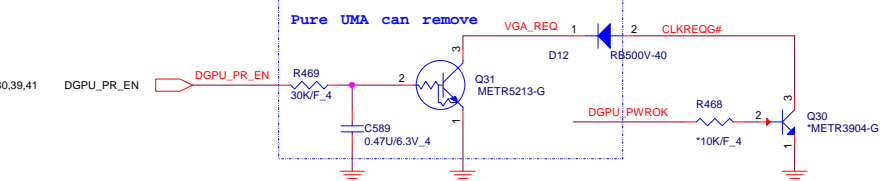
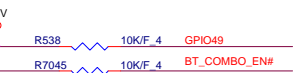
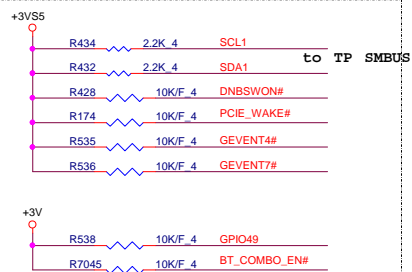
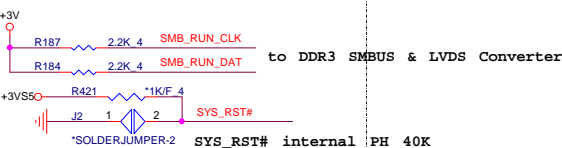
APU\_TEMP690 B20  
APU\_TEMP691 B19  
APU\_TEMP692 B18  
APU\_TEMP693 B16

APU\_TEMP694 D29  
APU\_TEMP695 D31  
APU\_TEMP696 D35  
APU\_TEMP697 D33  
APU\_TEMP698 D27  
APU\_TEMP699 D25  
APU\_TEMP700 D23  
APU\_TEMP701 D21

APU\_TEMP702 D19  
APU\_TEMP703 D17  
APU\_TEMP704 D15  
APU\_TEMP705 D13  
APU\_TEMP70



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted. FCH JTAG pins are overloaded for multiple functions, in this configuration the FCH JTAG are used as non-JTAG pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAG multi-function pins are configured as JTAG pins, in this configuration the FCH TAP can be accessed from FCH JTAG pins
1	TMS	1	Use on ATE only Yuba JTAG enabled



## BOARD ID SETTING

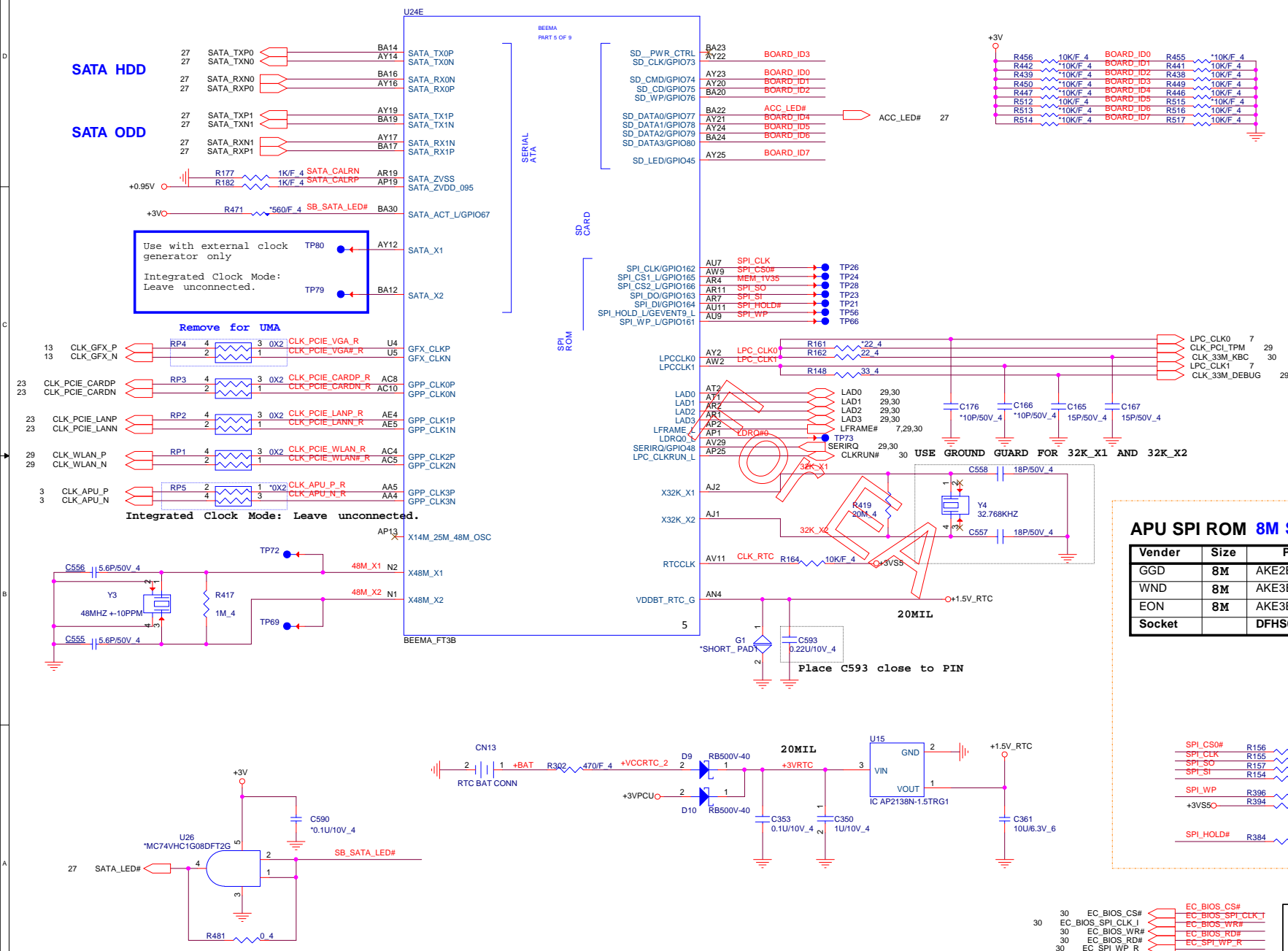
Board ID [0]	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14"
01	15"
10	17"

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve

Board ID [5]	Definition
0	Beema
1	Carrizo-L

Board ID [7:6]	Definition
000	Reserve



**PROJECT : Y2x**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>SATA/CLK (4/6)</b>	1A
Date: Tuesday, November 18, 2014	Sheet 5 of 41	

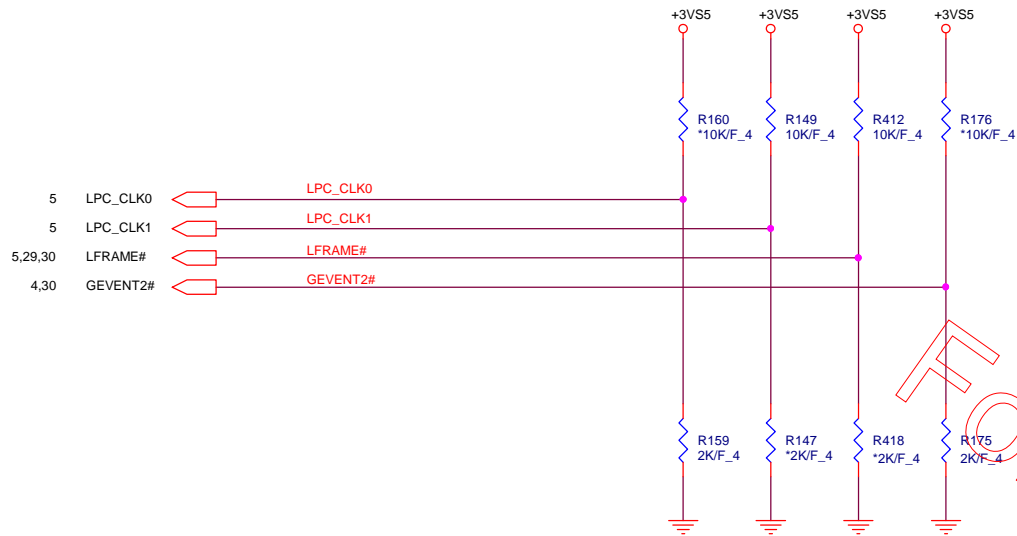




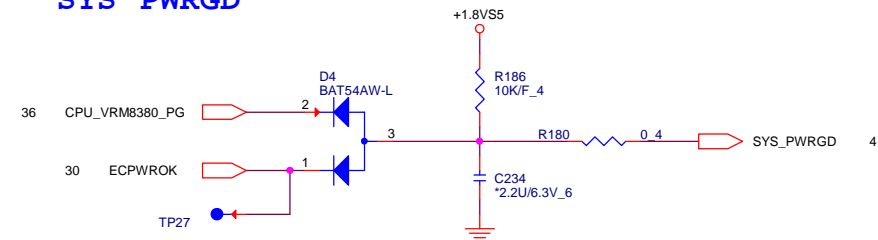


## STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.



## SYS\_PWRGD



## REQUIRED STRAPS


	LPC_CLK0	LPC_CLK1	LFRAME#	GEVENT2#
PULL HIGH	BOOT FAIL TIMER ENABLED	CLKGEN ENABLED DEFAULT	SPI ROM DEFAULT	1.8V SPI ROM
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	CLKGEN DISABLED	LPC ROM	3.3V SPI ROM DEFAULT



**PROJECT : Y2x**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>STRAP (6/6)</b>	1A
Date: Tuesday, November 18, 2014   Sheet 7 of 41		

For EA

	<b>PROJECT : Y71</b> Quanta Computer Inc.		
	Size B	Document Number <b>Reserved</b>	Rev 1A
	Date: Tuesday, November 18, 2014 Sheet 8 of 41		




For EA

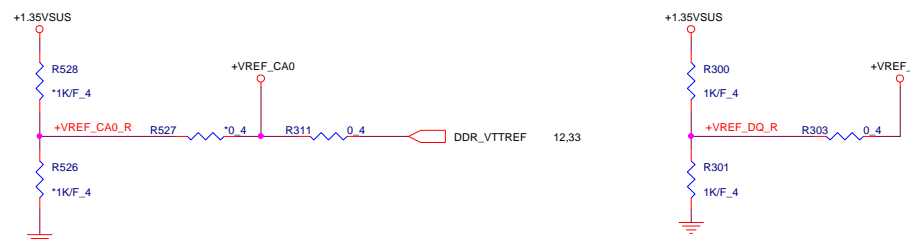
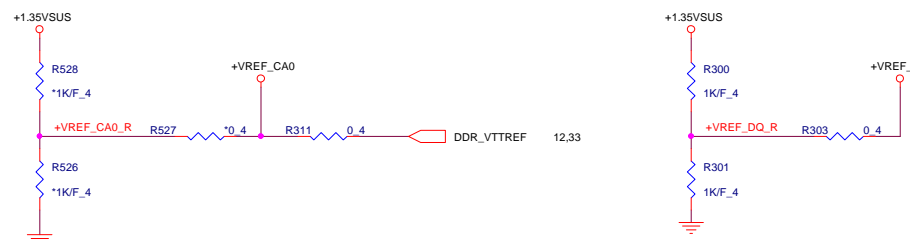
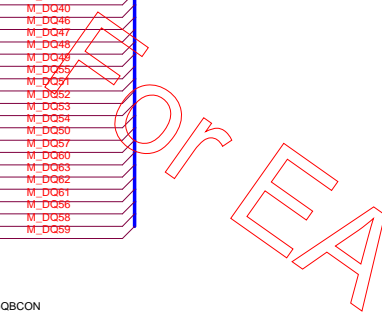


**PROJECT : Y71**  
Quanta Computer Inc.

Size B	Document Number Reserved	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 9 of 41		

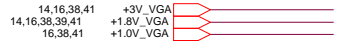
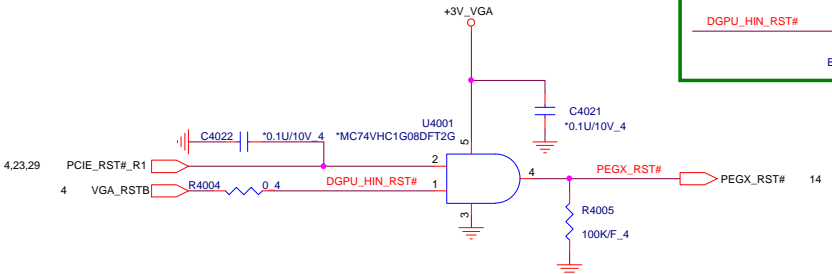
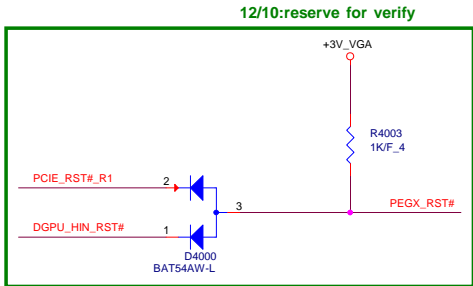
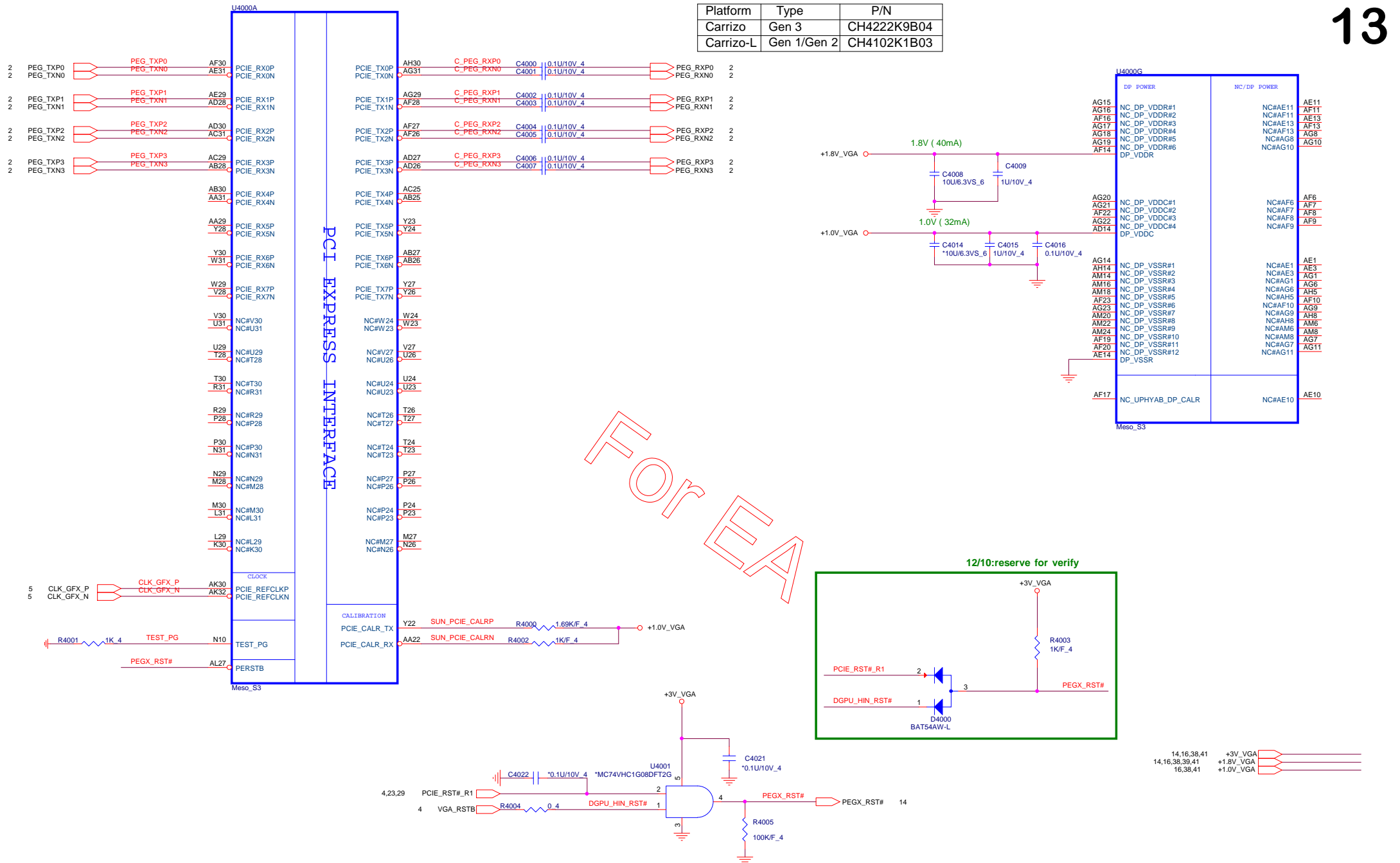
For EA

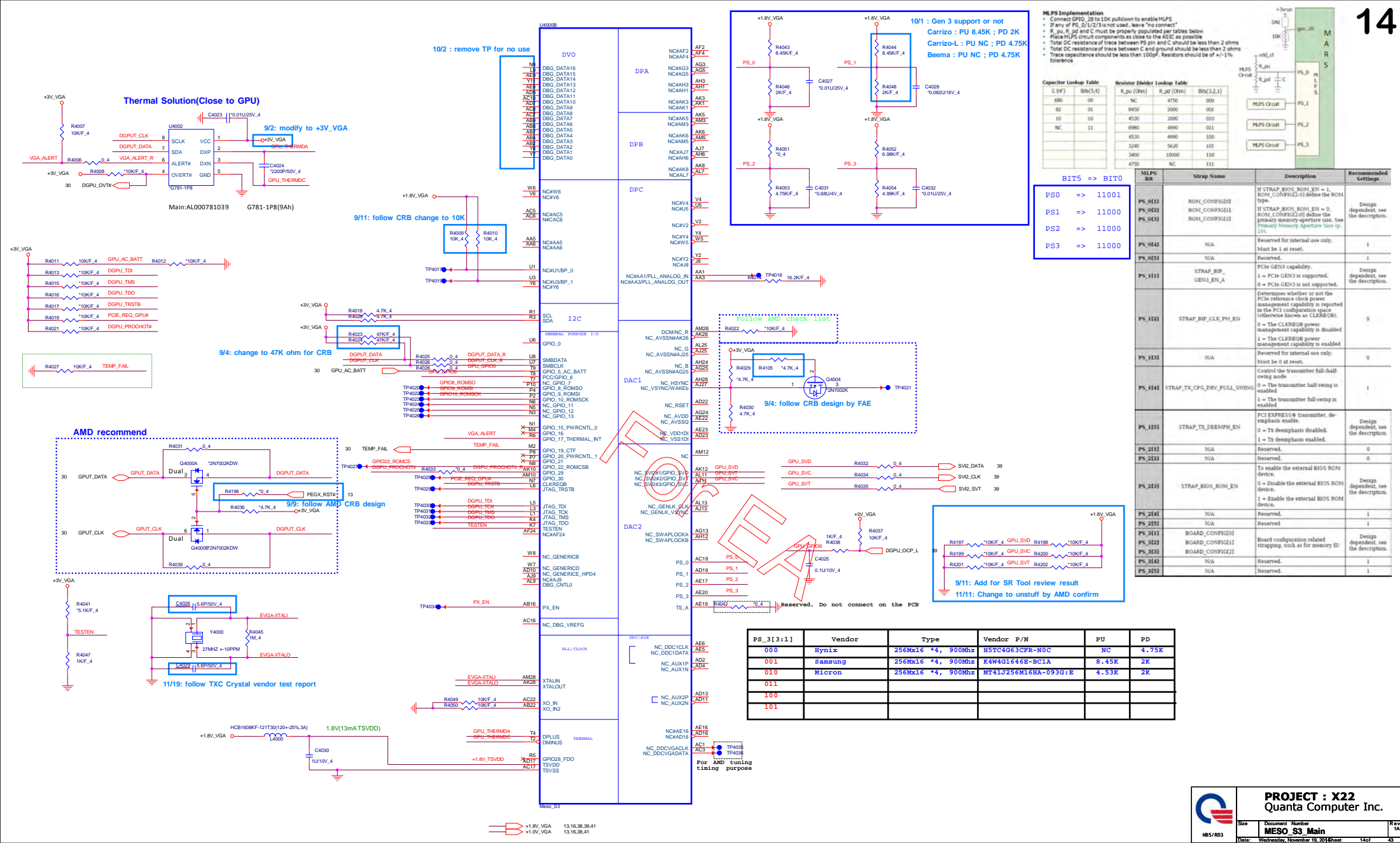
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	Size B	Document Number <b>Reserved</b>	Rev 1A
	Date: Tuesday, November 18, 2014		Sheet 10 of 41

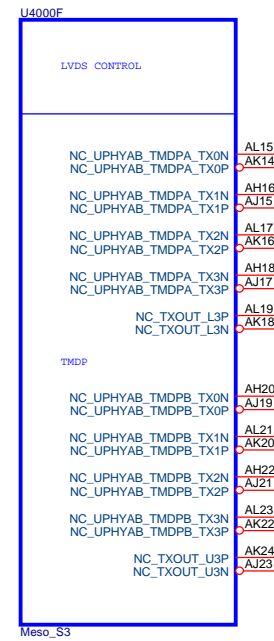
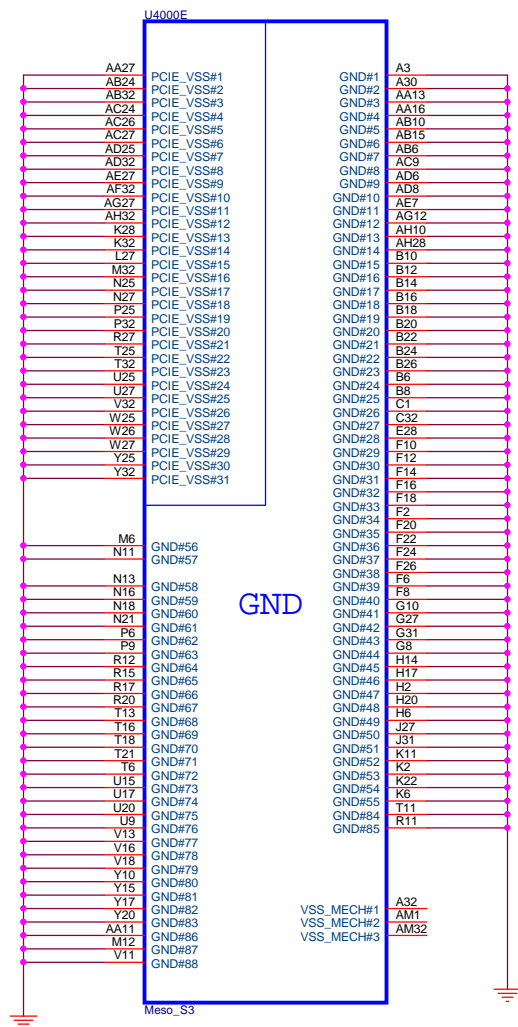




Platform	Type	P/N
Carrizo	Gen 3	CH4222K9B04
Carrizo-L	Gen 1/Gen 2	CH4102K1B03







### CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS  
0= DO NOT INSTALL RESISTOR  
1 = INSTALL 3K RESISTOR  
X = DESIGN DEPENDANT  
NA = NOT APPLICABLE

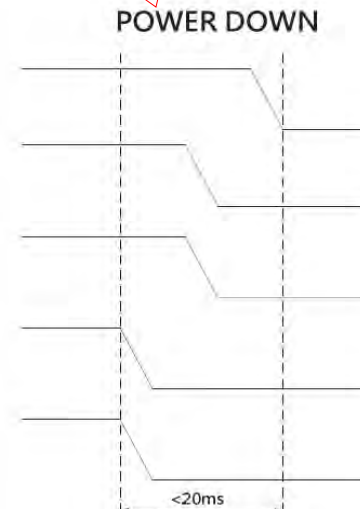
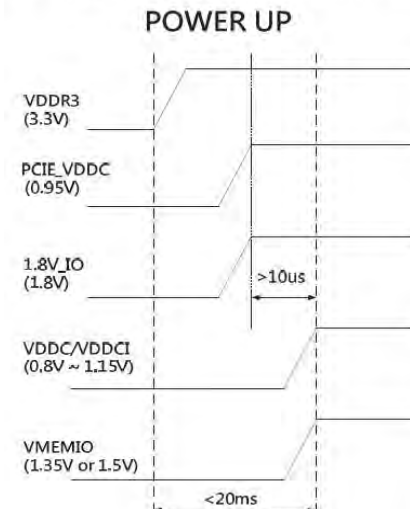
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	x
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA_DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1] AUD[0]	HSYNC VSYNC	SEE DATABOOK FOR DETAIL SEE DATABOOK FOR DETAIL	0 0
RSVD	GENERICC	RESERVED	0

### NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOs ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

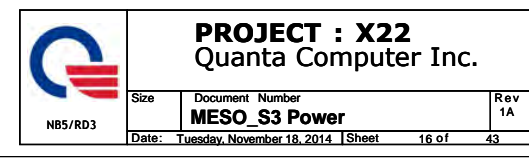
### POWER UP / POWER DOWN SEQUENCE

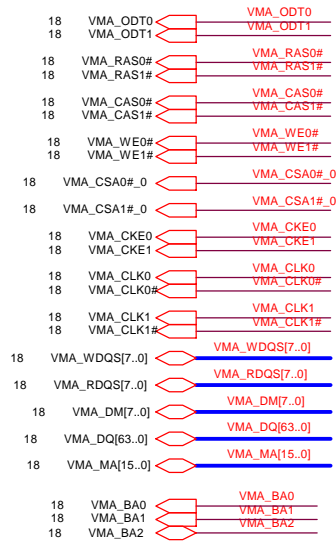


**PROJECT : X22**  
Quanta Computer Inc.

Size	Document Number	Rev
	<b>MESO_S3_GND/LVDS/Strap</b>	<b>1A</b>
Date:	Tuesday, November 18, 2014	Sheet 15 of 43

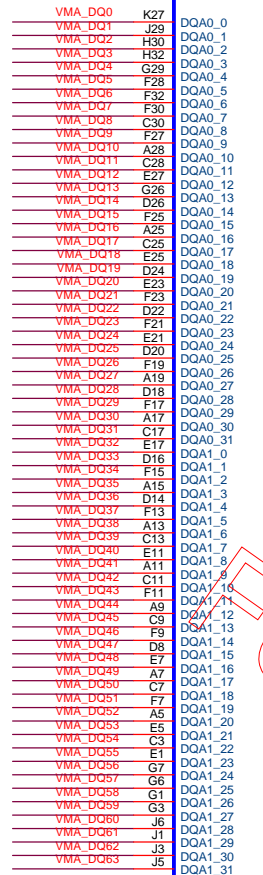




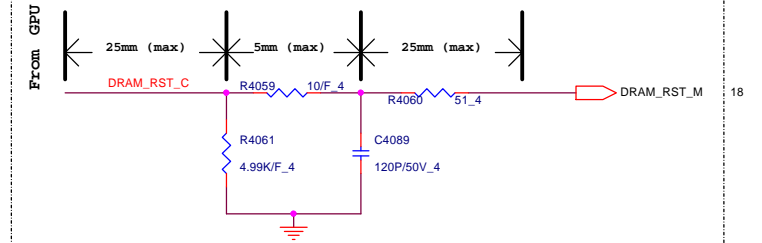
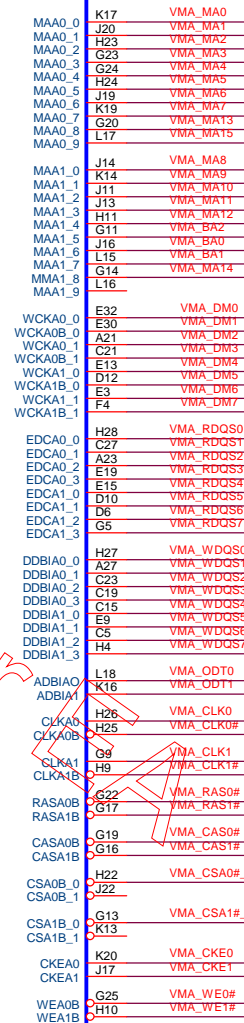


support 1Gbit  
VRAM ( 64M x 16 )

U4000C

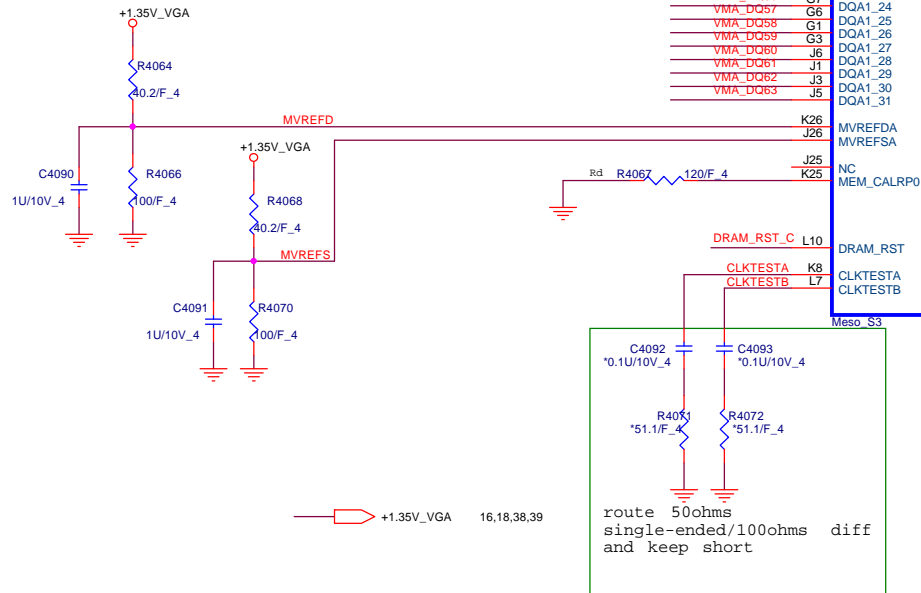


### MEMORY INTERFACE



Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM\_RST for DDR3/GDDR5. These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.




NB5/RD3

**PROJECT : X22**  
**Quanta Computer Inc.**

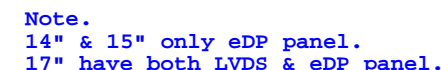
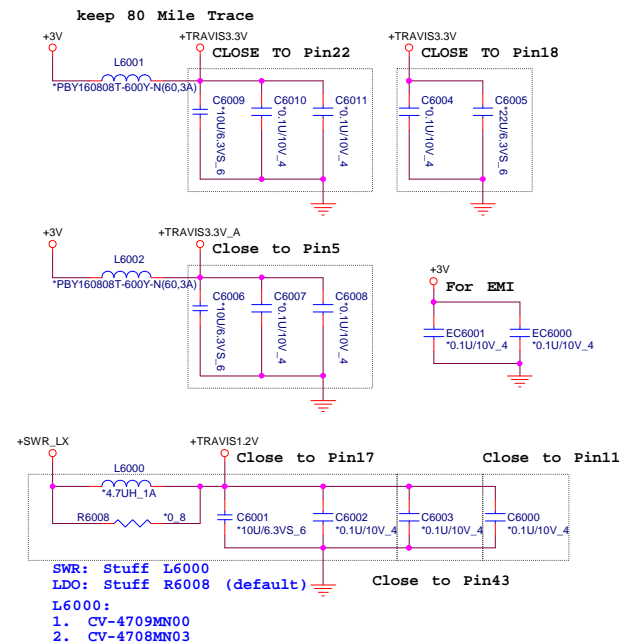
Size	Document Number	Rev
	<b>MESO_S3_MEM_Interface</b>	1A
Date:	Tuesday, November 18, 2014   Sheet	17 of 43



FOR EA

 NBS/RD3	<b>PROJECT : X22</b> Quanta Computer Inc.		
	Size Custom	Document Number <b>MESO S3 VRAM(DDR3 BGA96P)</b>	Rev 1A
	Date: Tuesday, November 18, 2014   Sheet 18 of 43		

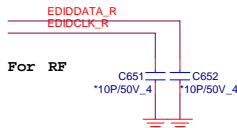
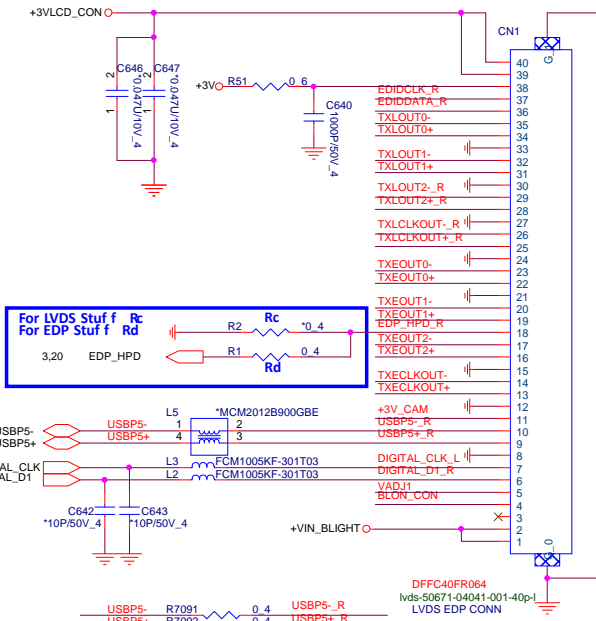
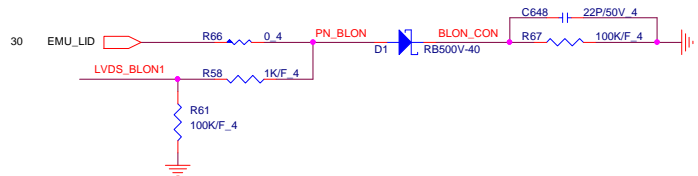
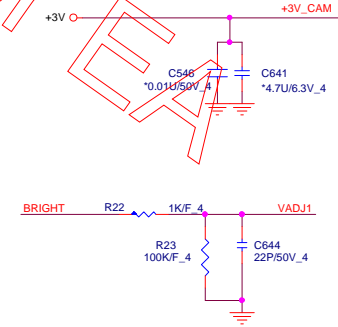
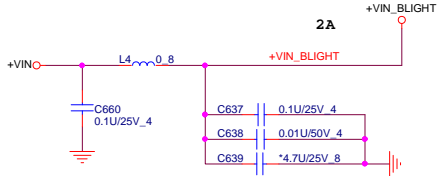
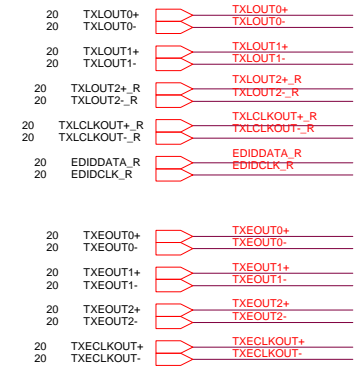
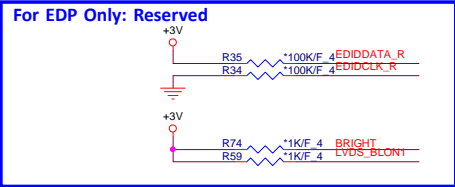
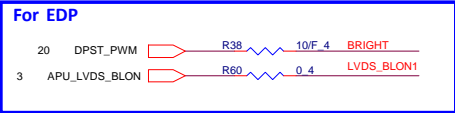
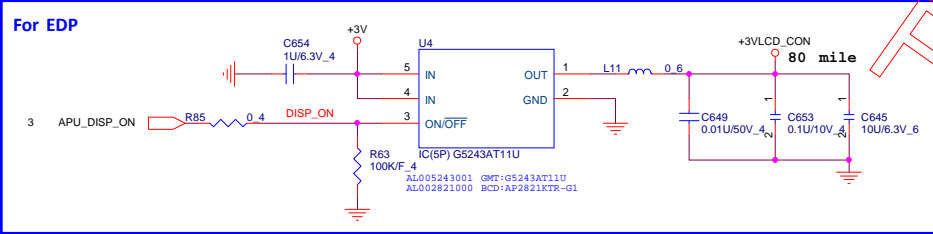
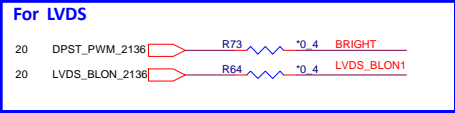
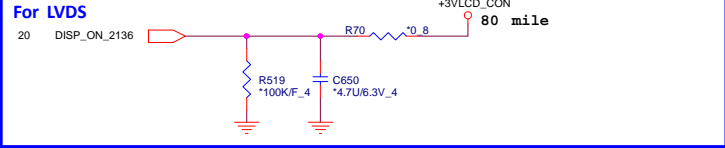
Pine 18: keep 80 Mile Trace

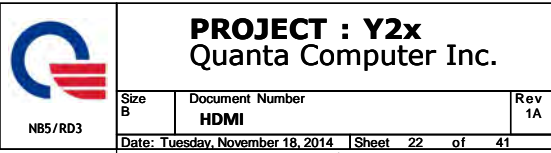


**WWW.AliSaler.Com**

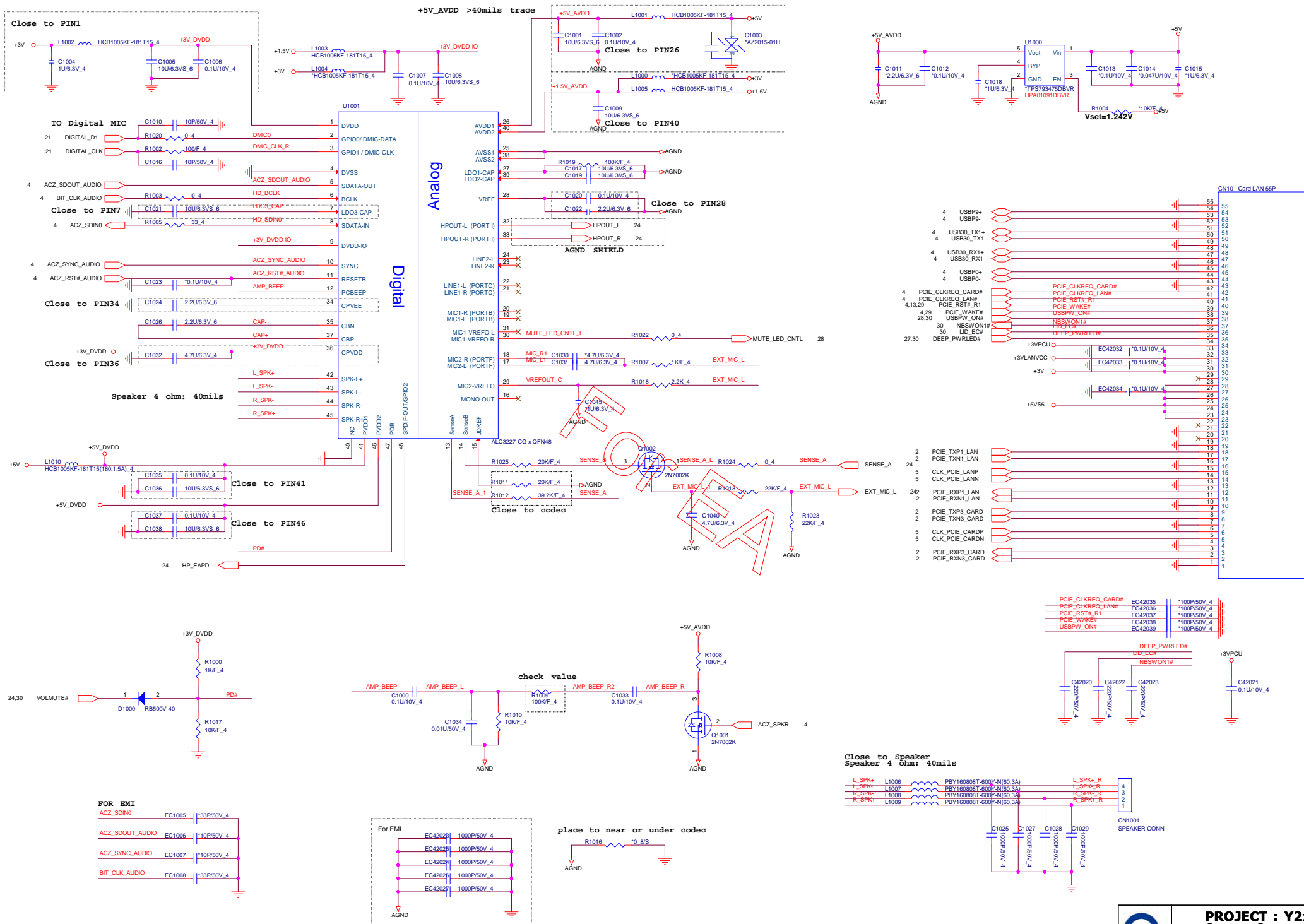
LVDS CONN.

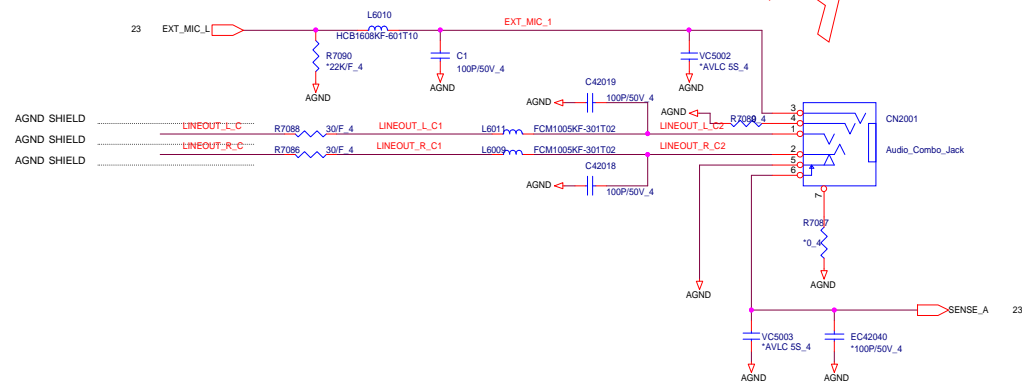
Note.  
14" & 15" only eDP panel.  
17" have both LVDS & eDP panel.



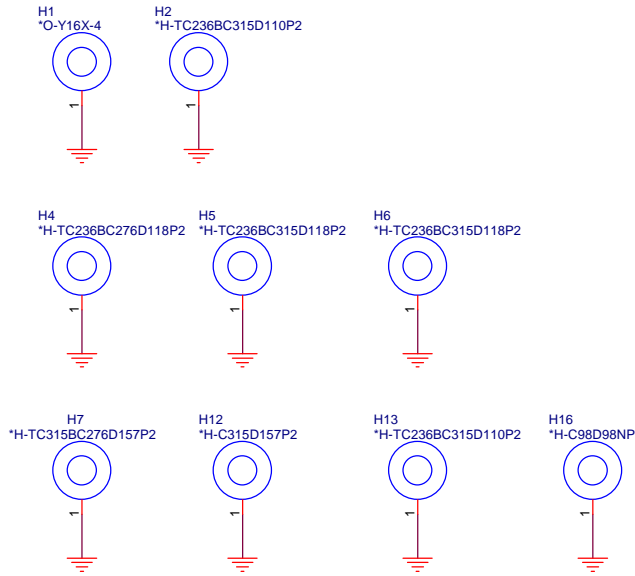




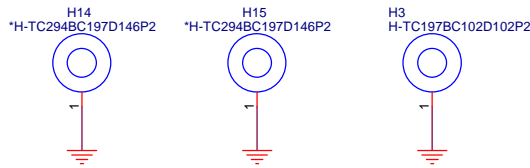




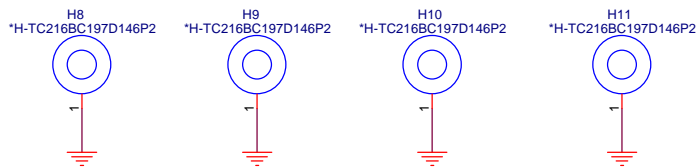
## Holes



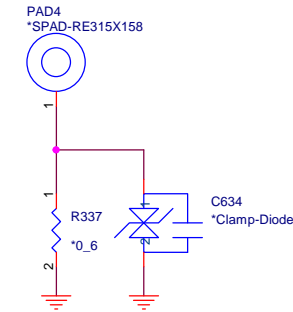
## GPU HOLES



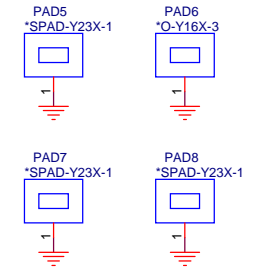
## APU HOLES



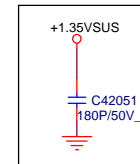
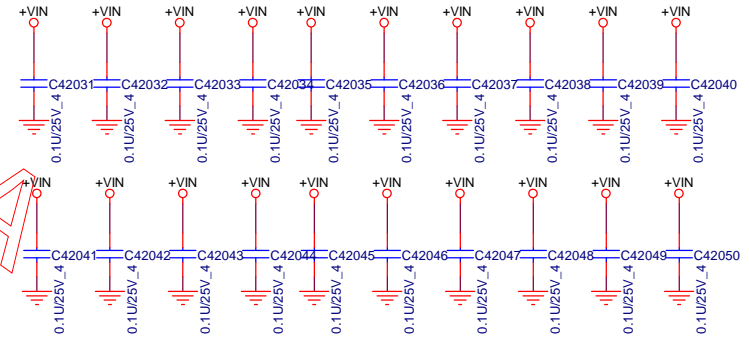
## Metal ESD



## EMI



Place on +VIN path




11/17 EMI request



**PROJECT : Y2x**  
Quanta Computer Inc.

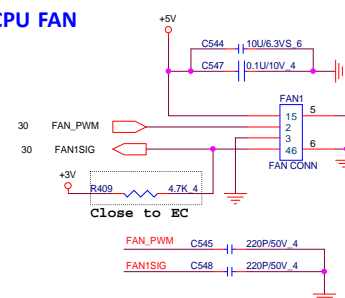
Size B	Document Number	Rev
	<b>Holes / EMI</b>	1A
Date: Tuesday, November 18, 2014	Sheet 25 of 41	

For EA

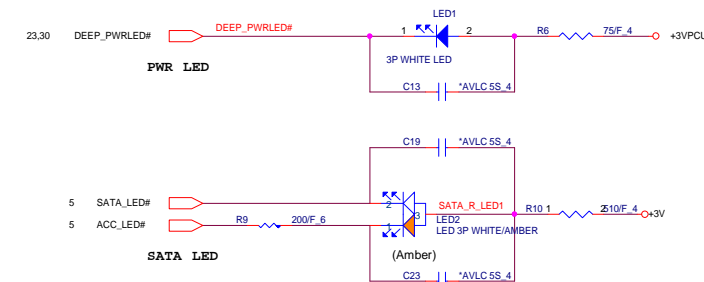
 NB5/RD3	<b>PROJECT : Y2x</b> Quanta Computer Inc.		
	Size B	Document Number <b>Reserved</b>	Rev 1A
	Date: Tuesday, November 18, 2014    Sheet    26 of    41		

## Power But t on Connect or ( Momet o DB)

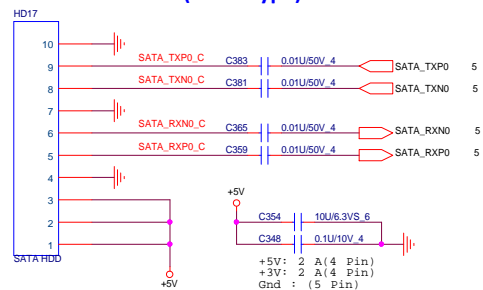
## CPU FAN



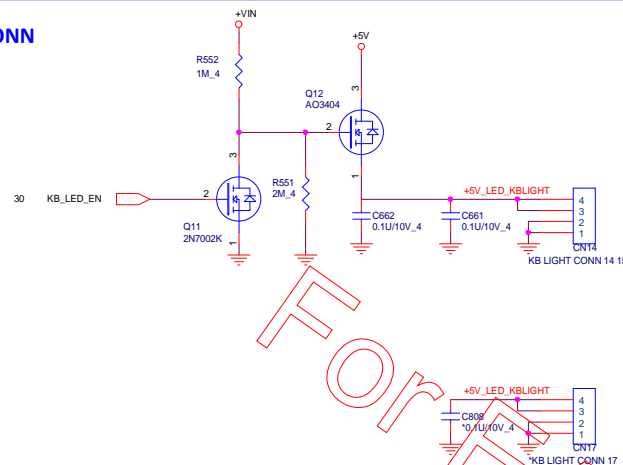
## LED



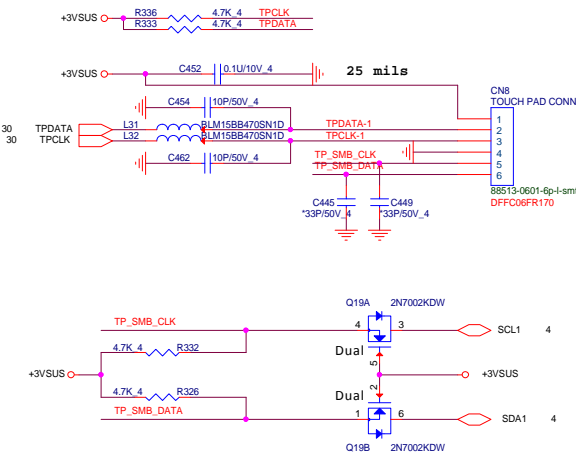
## SATA HDD CONN (Cable type)



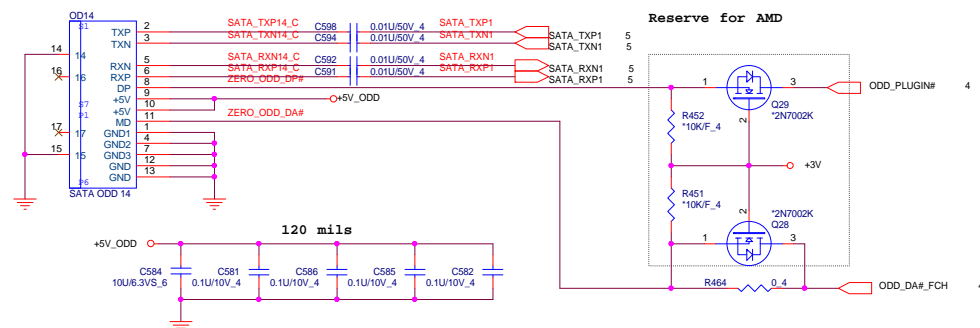
## KB LIGHT CONN



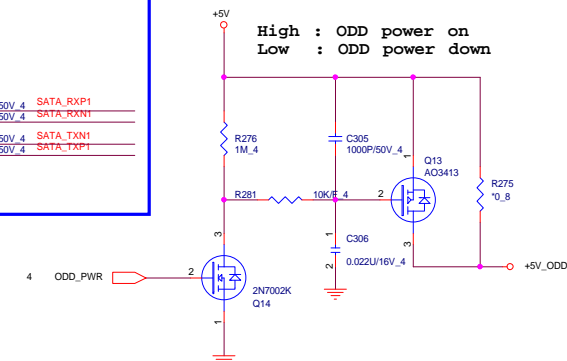
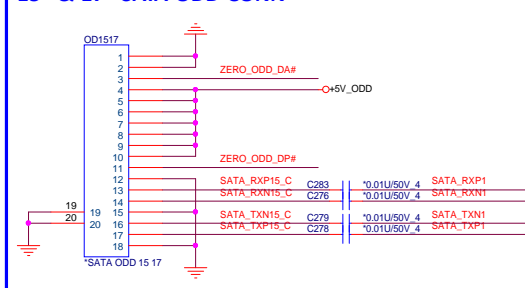
## Touch Pad



## 14" SATA ODD CONN

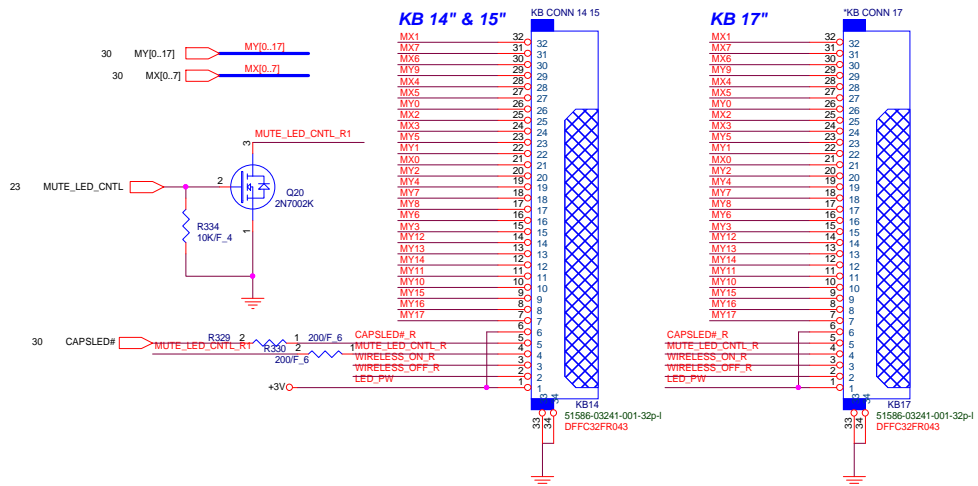


## 15" &amp; 17" SATA ODD CONN

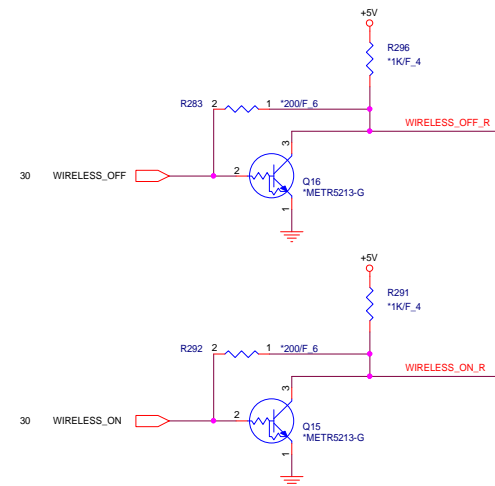
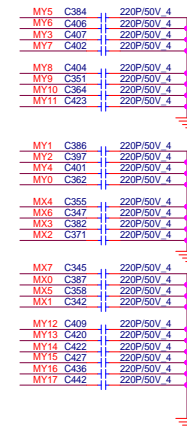
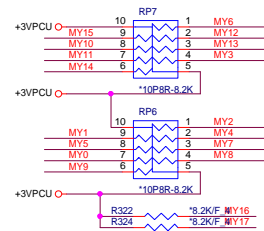


**PROJECT : Y2x**  
**Quanta Computer Inc.**

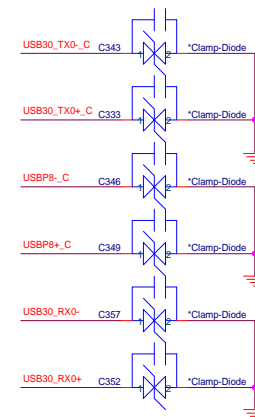
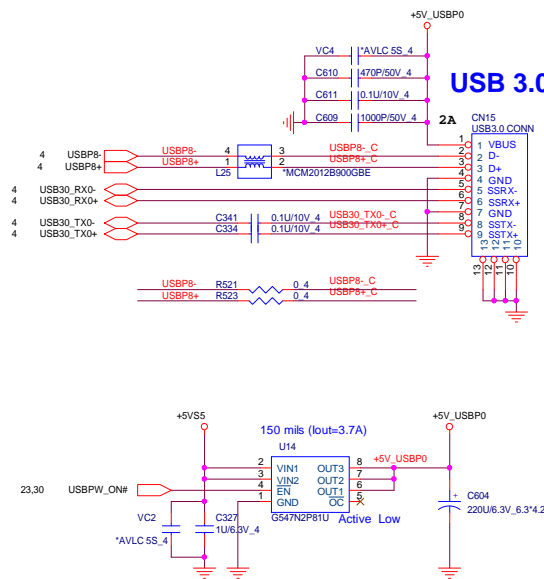
Size	Document Number	Rev
Custom	HDD/ODD/TP/FAN/LID/LED	1A
Date: Tuesday, November 18, 2014	Sheet 27 of 41	

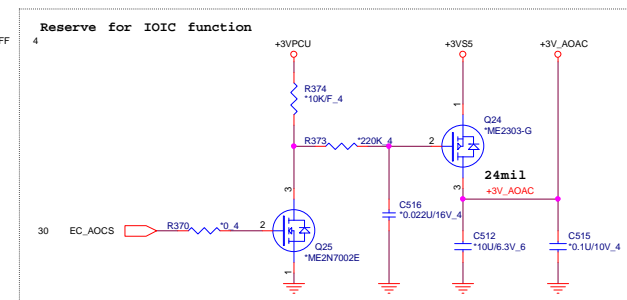
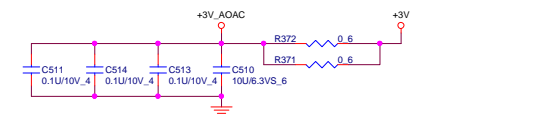
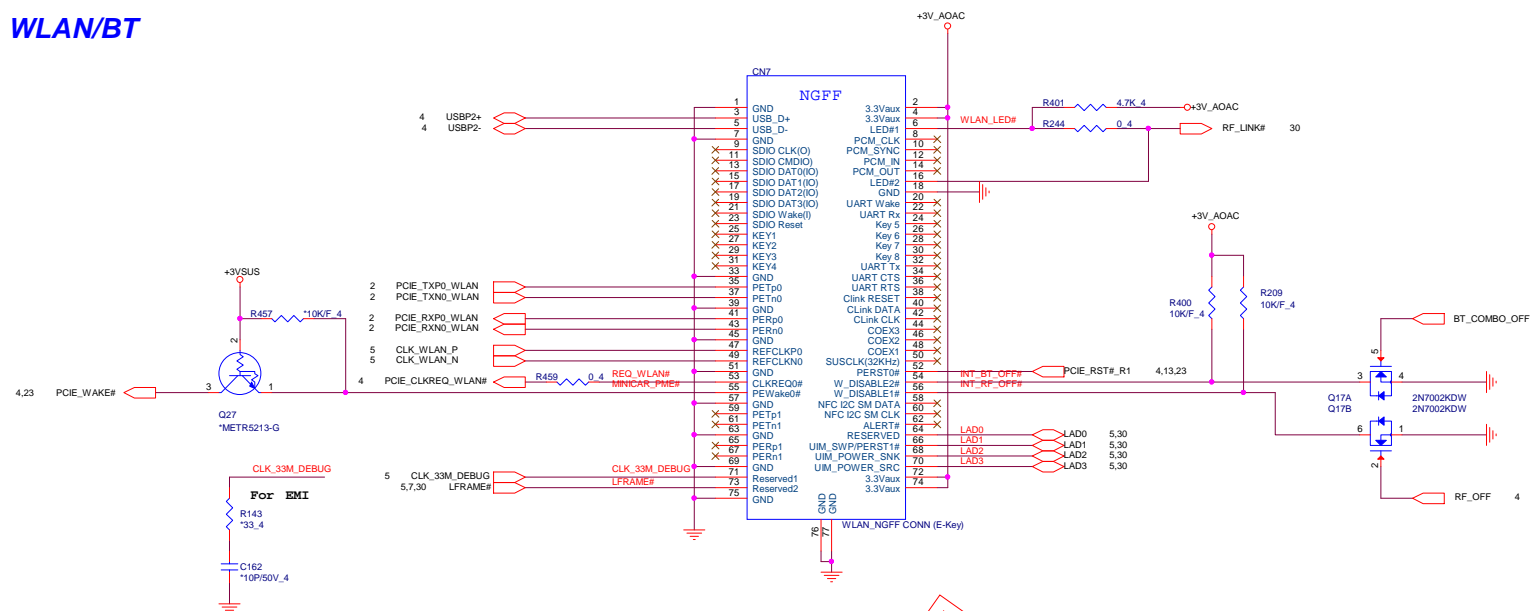


KEYBOARD PULL-UP

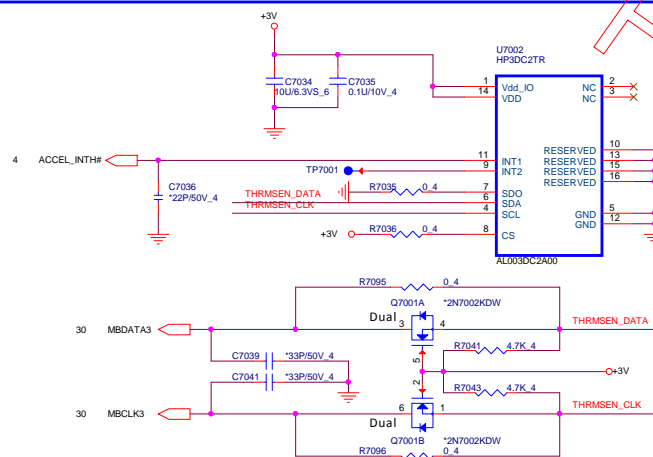


Left USB 2.0/3.0 Combo

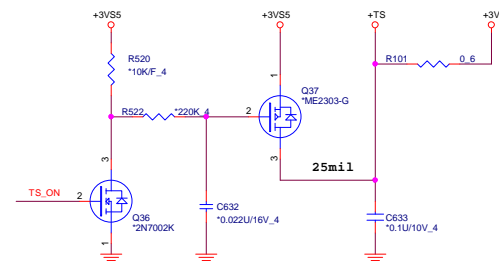
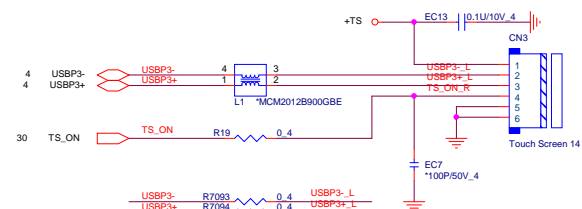




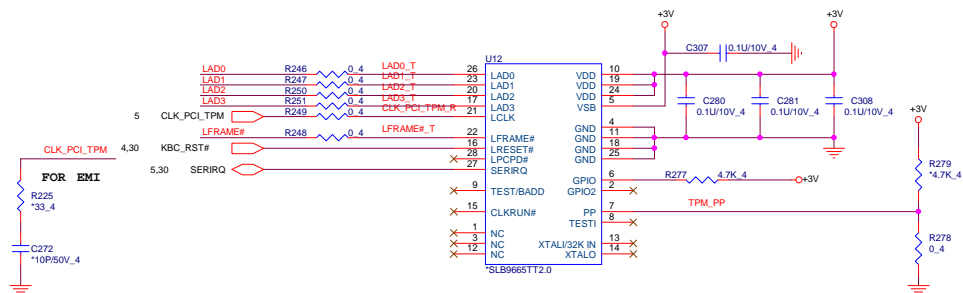
## Accelerometer Sensor



## Touch screen

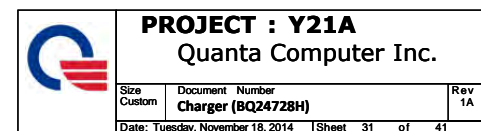


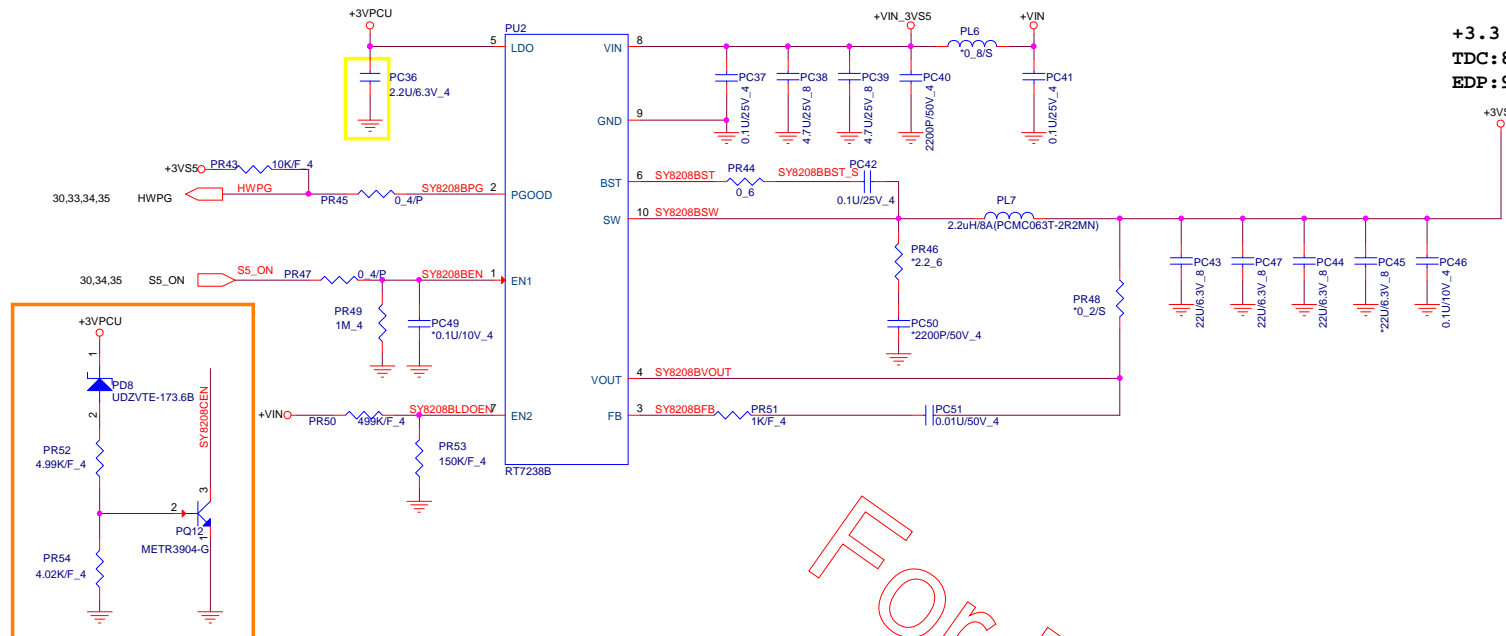
## TPM (2.0)



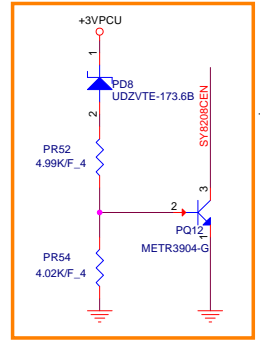




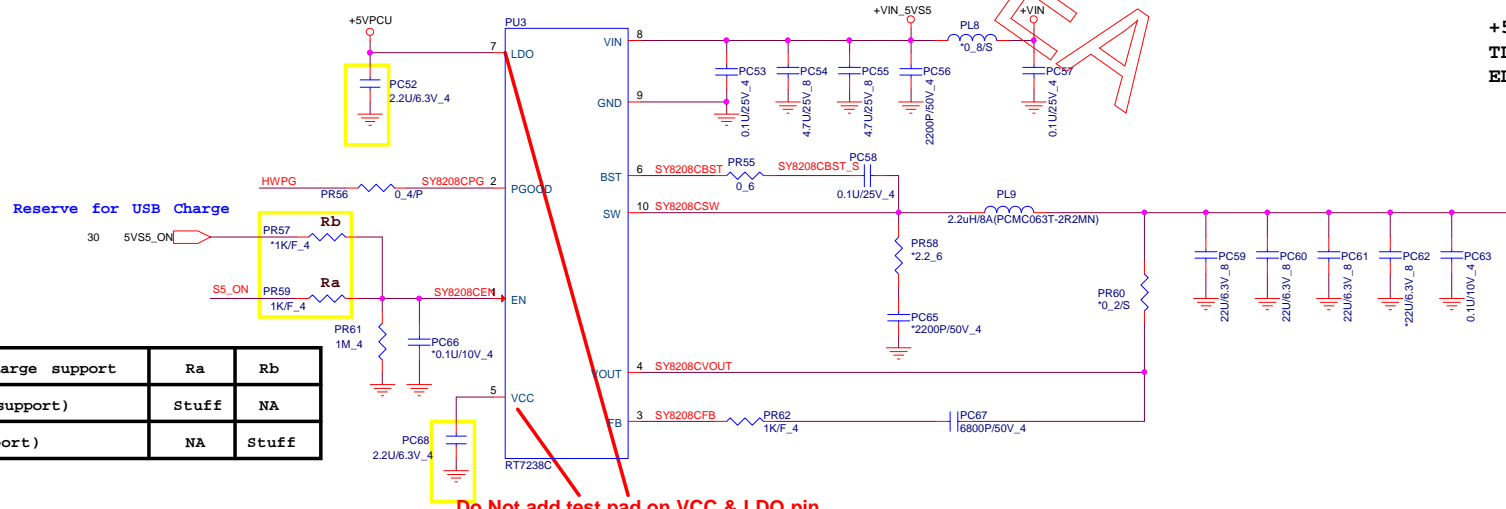




**+3.3 Volt +/- 5%**  
**TDC:8A**  
**EDP:9A**



Reserve



**+5 Volt +/- 5%**  
**TDC:8A**  
**EDP:9A**

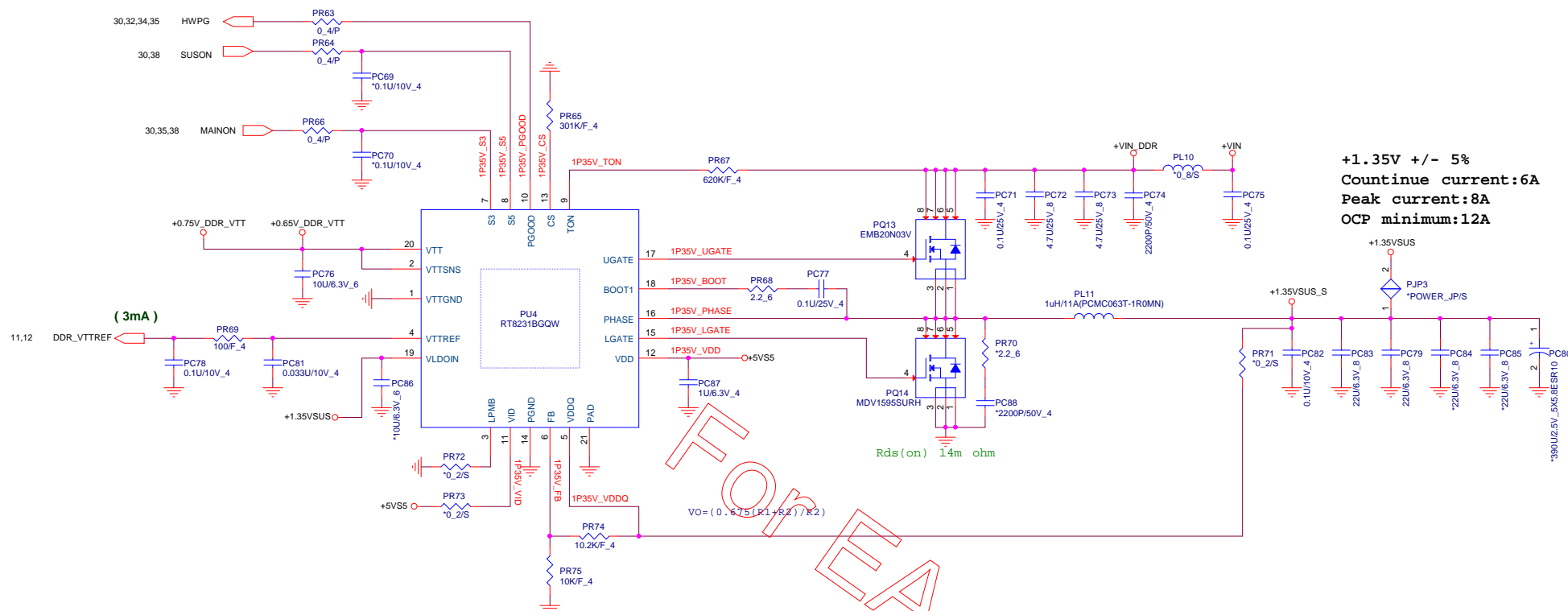
Reserve for USB Charge

USB Charge support	Ra	Rb
(No support)	Stuff	NA
(Support)	NA	Stuff

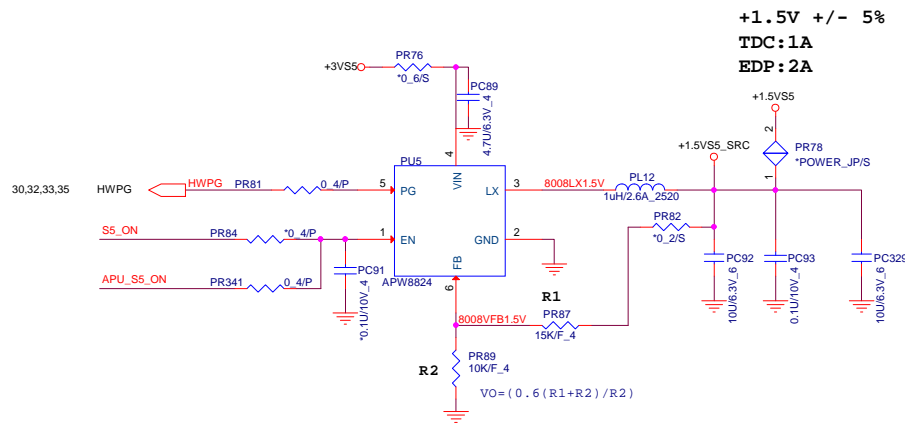
Do Not add test pad on VCC & LDO pin

**PROJECT : Y21A**  
**Quanta Computer Inc.**

Size Custom	Document Number 3/5VPCU(SY8208B/SY8208C)	Rev 1A
Date: Tuesday, November 18, 2014	Sheet 32 of 41	



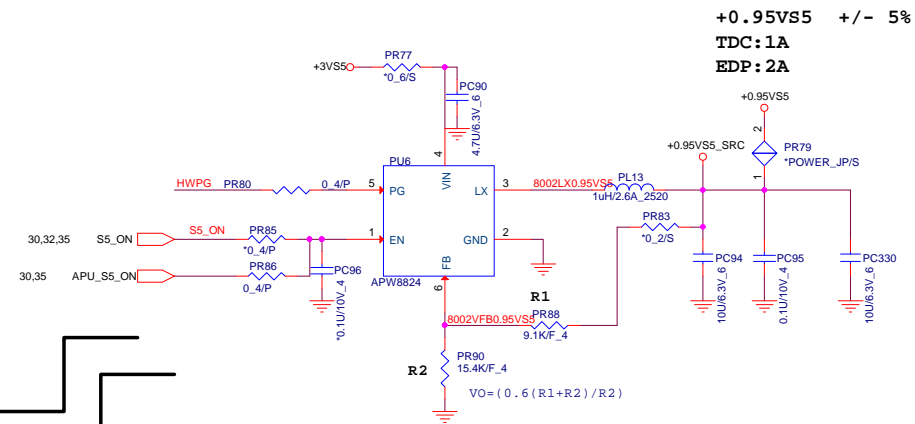
 +1.35VSUS 2,6,11,12,25




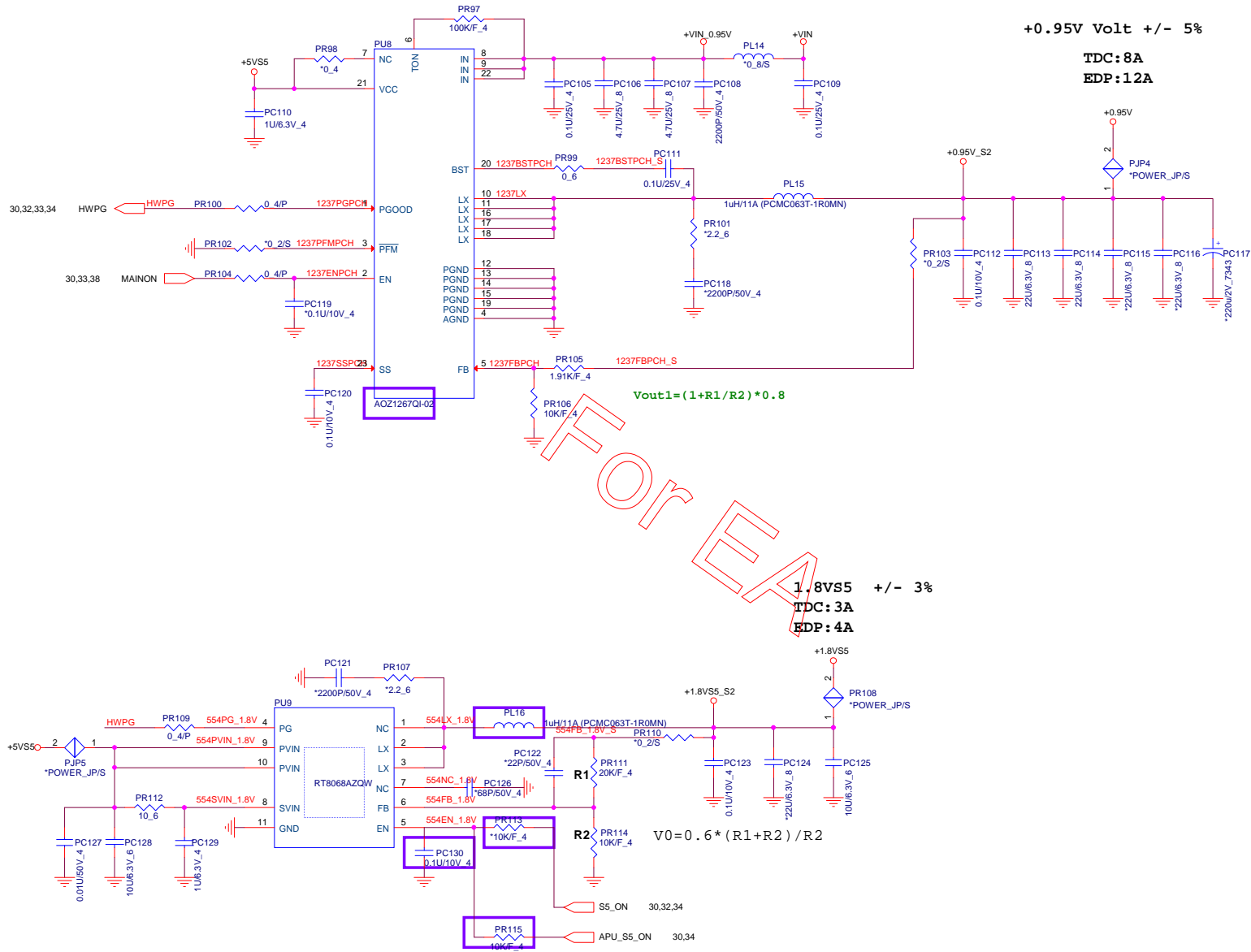
S5\_ON

APU\_S5\_ON

FOR EA



 <b>PROJECT : Y21A</b> Quanta Computer Inc.		
Size Custom	Document Number <b>+1.1VS5 (RT8228)/2.5V</b>	Rev 1A
Date: Tuesday, November 18, 2014 Sheet 34 of 41		

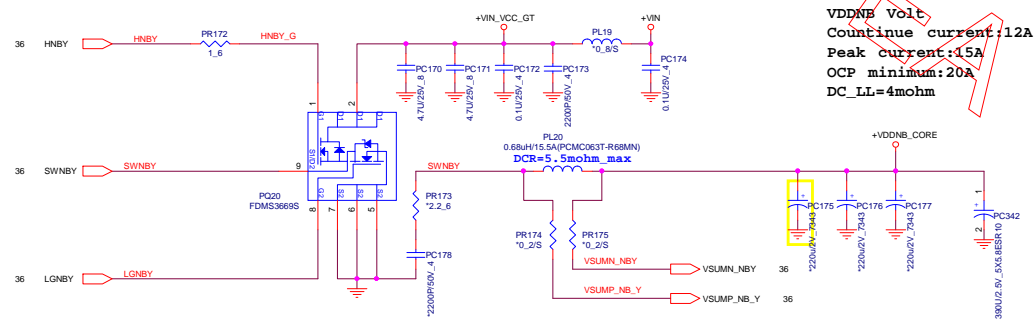
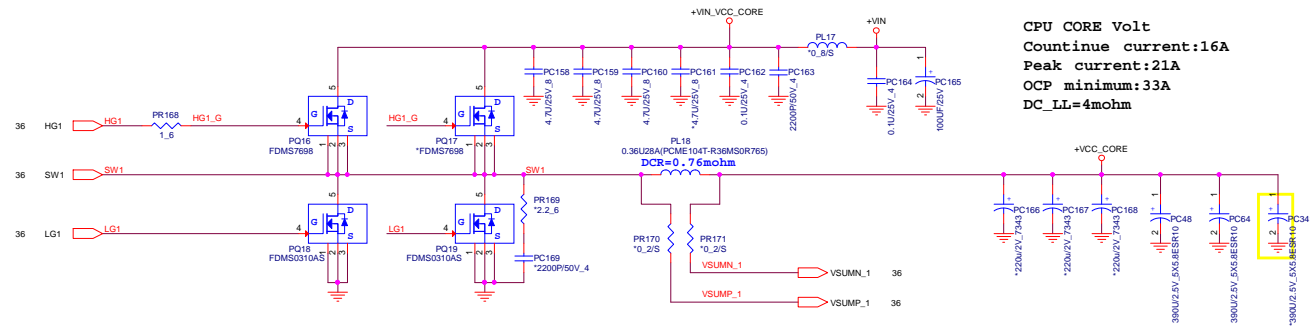


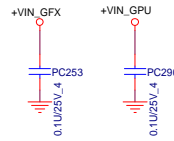
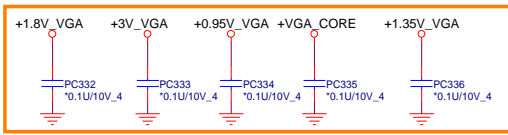
**PROJECT : Y21A**  
**Quanta Computer Inc.**

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Tuesday, November 18, 2014   Sheet 35 of 41		

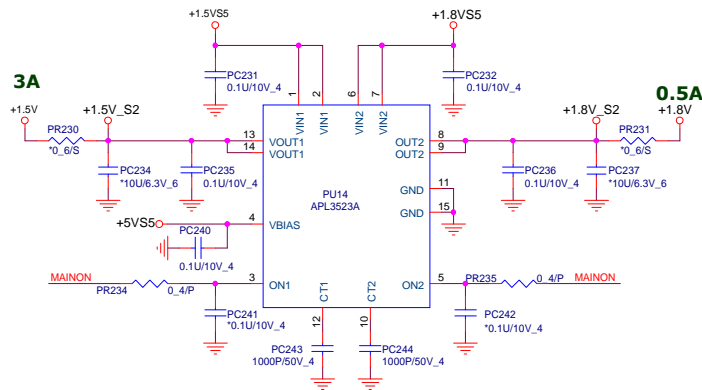
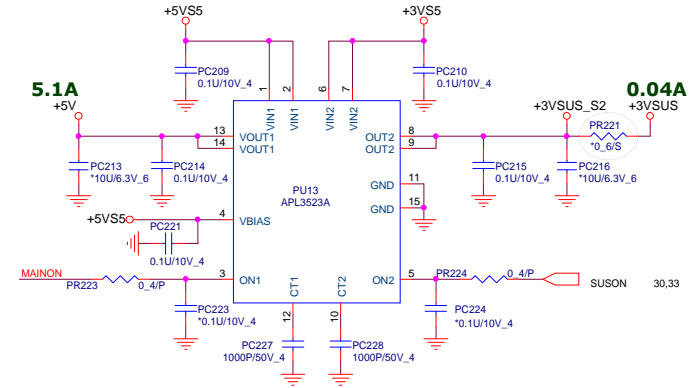
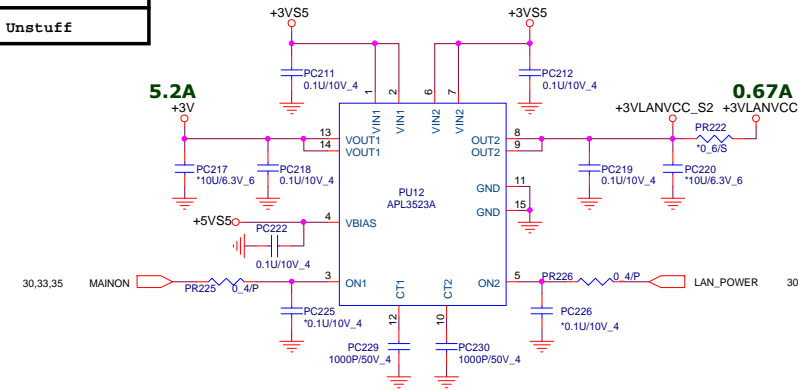






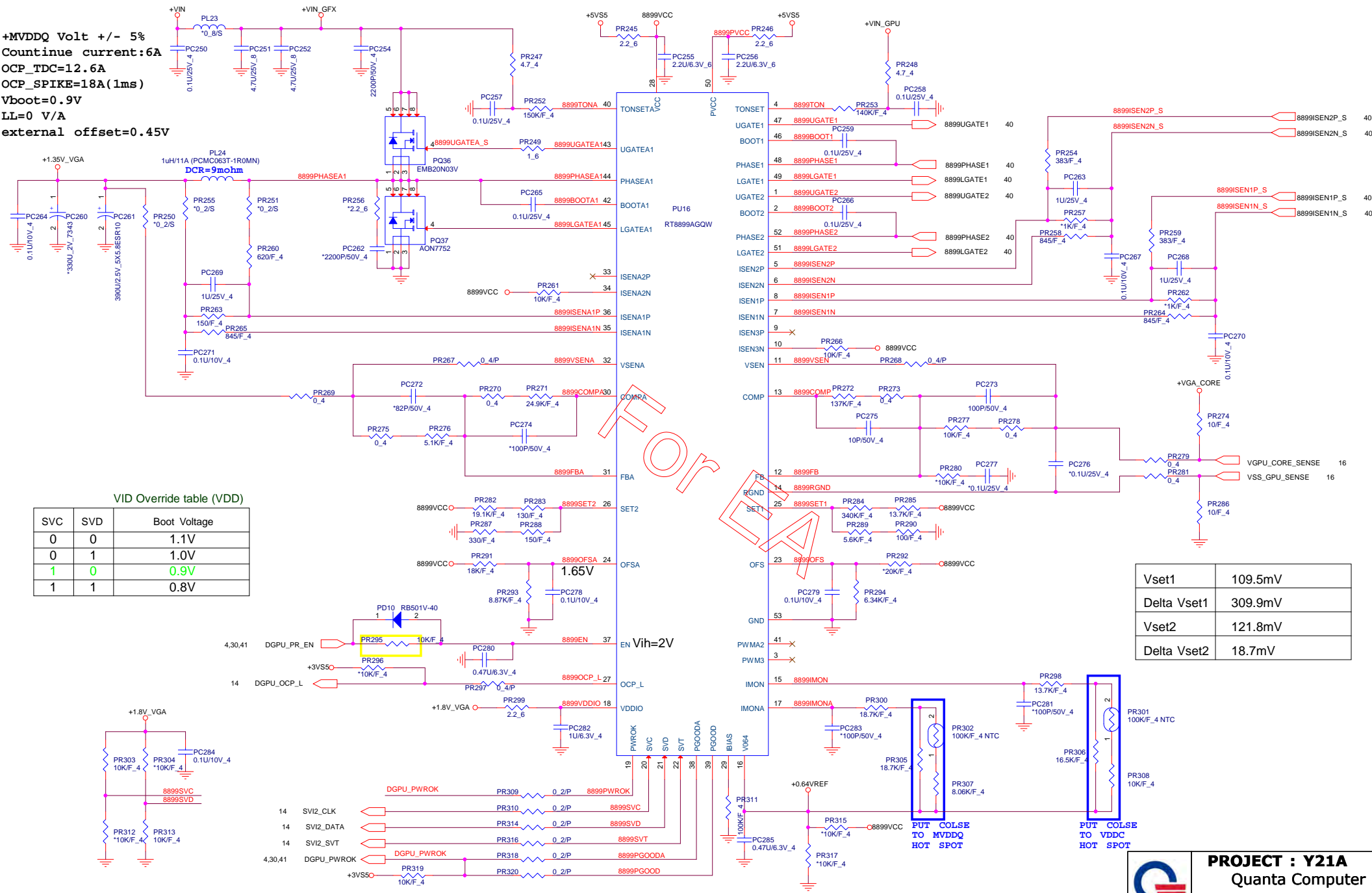


UMA only	Stuff
discrete	Unstuff




FOR EA

```
+MVDDQ Volt +/- 5%
Continue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V
```



SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

	<b>PROJECT : Y21A</b> <b>Quanta Computer Inc.</b>		
	Size Custom	Document Number Vcore (RT8899A)	Rev 1A
	Date: Tuesday, November 18, 2014		Sheet 39 of 41

